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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,127	07/27/2001	Larry D. Kinsman	3572.1US (97-1243.1)	3326

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TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 10/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/917,127	KINSMAN ET AL.	
	Examiner	Art Unit	AW
	Michael Trinh	2822	

-- The MAILING DATE of this communication app ars on th cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6 and 11-29* is/are pending in the application.

4a) Of the above claim(s) *19,20 and 25-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,11-18,21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *13,14* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's amendment filed on July 11, 2003. Claims 5,7-10 were canceled. Claims 1-4,6,11-29, in which claims 19-20, 25, and 26-29 are non-elected, without traverse.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

1. Claims 1-4,6,11-18,21-24 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention, and as failing to comply with the enablement requirement, in which the claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Base amended claim 1, last step, recites "... forming a layer of encapsulant material over substantially all of the active surface and into said channels such that a surface of said layer of encapsulant material has a pattern of depressions over said channels and a portion of said at least one intermediate conductive element is exposed through and coplanar with said surface of said layer of encapsulant material...".

However, the specification including paragraph [0033] does not describe how to do it and in such a way as to reasonably convey to one skilled in the art in such way as to enable one skilled in the art to make the invention so as to the surface of the encapsulant having a pattern of depression over the channels, as shown in Figure 2, wherein the intermediate conductive element is coplanar with the surface of the encapsulant material. As contradictorily shown in Figures 1B-1F, there is showing a similar structure, but the encapsulant material 30 does not include a pattern of depressions formed over the channels, wherein the encapsulant material is planar and formed over the entire surface of the substrate. As can be seen, specification including paragraph [0033] just describes a product of Figure 2 having a pattern of depression over the channels, but it fails to teach how to do it in such a way enable to make the claimed invention.

(Dependent claims are rejected as depending on rejected base claim)

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-3,6,12,14,17,21,23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Uemura (6,331,450).

Uemura teaches a method for forming a semiconductor device comprising at least the steps of: providing a semiconductor substrate 10 having an active surface including at least a layer of integrated circuit, with a plurality of die (Figs 2F,3D,1), with plurality of bond pads 120,140 with each die; forming intermediate conductive elements 220 over the bond pads to project a height over the active surface; forming a pattern of mutually traverse recess channels to depth below the layer and circumscribing a die and exposing peripheral edges of the circuit device (Figs 2A-3D,1; col 5, lines 25-40), wherein the channels have parallel sidewalls (re claim 6); forming a layer of encapsulant material over substantially all of the active surface and into said channels such that a surface of said layer of encapsulant material has a pattern of light depressions over said channels due to the recess channels, and a portion of said at least one intermediate conductive element is exposed through and coplanar with said surface of said layer of encapsulant material 230,210 (Figs 2A-2F; 3A-3D; col 5, line 47 through col 7, line 16). *Re claim 2*, wherein an external conductive elements 240 is formed over the intermediate conductive elements 220 (Figs 2E-2F;3D). *Re claims 3 and 23*, the method further comprises severing the substrate in alignment with the channels into a plurality of semiconductor elements, each element comprised of at least one individual die location, wherein the exposed peripheral edges of the integrated circuitry remain covered with the encapsulant material 230 (Figs 2E-2F; col 6, lines 7-

25). *Re claim 6*, wherein the recess channels (Figs 2A-2F) have parallel sidewalls. *Re claim 12*, wherein the conductive elements 220 comprises pillars of conductive copper (col 5, lines 52-65; col 6, lines 45-58); Figs 2B-2C). *Re claim 14*, wherein external conductive elements 240 comprises solder balls (Figs 2E-2F; col 6, lines 1-12). *Re claim 17*, wherein the encapsulant material 230 is resin material of polyester resin, polyimide resin, phenolic resin, polyurethane resin, silicone resin, and thermosetting resin (col 5, lines 62-67; col 6, lines 50-55). *Re claims 21 and 24,* wherein the intermediate conductive element in alignment with one conductive bump including a terminal pads and "external members" protruding from a carrier 6 (Figs 6-6C; col 1, line 27 through col 2, line 15); and electrically connecting the conductive element 1 to the conductive bump, *re further claim 24,* wherein one external conductive element 240 is placed on the intermediate conductive element 220 (Figs 2E-2F; 3C-3D) .

Claim Rejections - 35 USC § 103

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uemura (6,331,450), and further of Abe et al (4,610,079).

Uemura teaches a method for forming a semiconductor device as applied to claims 1-3, 6,12,14,17,21,23-14 above.

Uemura shows the channels having U-shape with parallel sidewalls, as similarly recited in claim 6, while claim 4 alternatively recites the channels having sloped sidewalls.

Abe teaches forming in the wafer dicing lines of either U-shaped channel having parallel sidewalls (Fig 2a) or V-shaped channel having sloped sidewalls (Fig 2b; col 2, lines 19-54).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the channels of Uemura to have a U-shape or V-shape as taught by Abe, because channels of either shape facilitate easy dicing and breaking of the wafer into a plurality of individual dies, wherein these channels are art recognized equivalent and alternative for substitution as scribe lines.

5. Claims 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uemura (6,331,450) taken with Chakravorty (6,181,569).

Uemura teaches a method for forming a semiconductor device as applied to claims 1-3, 6,12,14,17,21,23-24 above.

Re claims 11 and 13, Ohuchi forms the intermediate conductive elements 4 of pillar posts, but lacks mentioning forming the conductive elements as solder ball by wire bonding.

However, Chakravorty teaches (at col 8, line 57 through col 9; col 13, lines 35-62;) several alternative processes for forming on the bond pad the intermediate conductive elements (311,322,323, 325,326 in Figs 5a,6,8d,10c-g) having the shape of pillar bump and solder balls, wherein wire bonding capillary is used for forming the conductive elements (col 9, lines 10-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the conductive elements of Ohuchi by employing several established techniques including wire bonding capillary for solder balls as taught by Chakravorty, because these established techniques are alternative and art recognized equivalent for forming a conductive elements on the bond pads, wherein different shapes of the conductive elements depend on the process of their formation.

6. Claim 17 is further rejected under 35 U.S.C. 103(a) as being unpatentable over Uemura (6,331,450) and further of Farnworth (5,933,713).

Uemura teaches a method for forming a semiconductor device as applied to claims 1-3, 6,12,14,17,21,23-14 above. Re claim 17, Uemura already teaches (at col 6, lines 50-55) forming a resin by using a material of polyester resin, polyimide resin, phenolic resin, polyurethane resin, silicone resin, and thermosetting resin.

Ohuchi thus teaches most resin for the encapsulant material (col 3, lines 25-35), but lacks mentioning other encapsulant materials including epoxies, silicone-carbon resin, glasses, etc., as recited in claim 17.

However, Uemura already teaches (at col 6, lines 50-55) forming a resin by using a material of polyester resin, polyimide resin, phenolic resin, polyurethane resin, silicone resin, and thermosetting resin. Farnworth '713 teaches (at Fig 5; col 6, lines 16-41) encapsulating the substrate with an encapsulant materials including polymers, epoxies, silicones, silicone-carbon resins, polyimides, polyurethanes, and glasses.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to encapsulate the substrate of Uemura by using other alternative encapsulant materials including polymers, epoxies, silicones, silicone-carbon resins, polyimides, polyurethanes, and glasses, as combinatively taught by Uemura and Farnworth '713. This is because of the desirability to encapsulate and protect the substrate, wherein these encapsulant materials are art recognized equivalent and alternative for substitution in encapsulating the wafer.

7. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uemura (6,331,450) and further of Brooks et al (5,824,569).

Uemura teaches a method for forming a semiconductor device as applied to claims 1-3, 6,12,14,17,21,23-14 above.

Re claim 18, Uemura lacks forming encapsulant material in the back of the substrate.

However, Brooks '569 teaches (at Figs 3-5) forming an encapsulant material 36A in the back of the substrate 30.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the method of Uemura by also encapsulating the back side of the substrate with an encapsulant material as taught by Brooks, because it would protect the back side of the substrate from contamination and damage.

8. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uemura (6,331,450) and further of Ohuchi (6,107,164).

Uemura teaches a method for forming a semiconductor device as applied to claims 1-3, 6,12,14,17,21,23-14 above.

Re claim 22, Uemura lacks bond pads over the conductive elements before electrically connecting to the bumps.

However, Ohuchi teaches (at Fig 6; col 6, lines 2-12) forming a bond pad 13 on exposed portions of the intermediate conductive elements 4 before electrically connecting to other external bumps.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the method of Uemura by forming bond pads on the intermediate conductive element as taught by Ohuchi, because of the desirability to prevent corrosion of the exposed surfaces of the intermediate elements before electrically connecting.

9. Claims 12 and 15 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Uemura (6,331,450) and Chakravorty (6,181,569), as applied to claims 11 and 13, and further of Farnworth (6,020,629).

Uemura teaches a method for forming a semiconductor device as applied to claims 1-3, 6,11-14,17,21,23-14 above, wherein the intermediate conductive elements 220 comprises pillars of conductive copper.

Uemura already teaches forming the conductive elements of conductive pillar post and solder balls while claims 12 and 15 further recites alternative materials for conductive elements including conductor filled epoxy, or a metal filled elastomer.

However, Ohuchi teaches the conductive elements 4 comprising pillars of conductive copper (col 2, lines 60-63). Chakravorty teaches (at col 8, line 57 through col 9; col 13, lines 35-62;) several alternative processes for forming the conductive elements (311,322,323, 325,326 in Figs 5a,6,8d,10c-g) having the shape of pillar bump and solder balls, wherein different shapes of the conductive elements depend on the process of their formation. Farnworth '629 teaches (at col 5, lines 1-11) forming a conductive elements by using metal, or conductive elastomer, such as epoxy or silicone with embedded metal particles.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the conductive elements of Ohuchi by employing pillars of conductive metal, conductor-filled epoxy, or metal filled elastomer, as combinatively taught by Ohuchi, Chakravorty, and Farnworth '629. This is because of the desirability to form the conductive elements for electrical connection, wherein these conductive materials are art recognized equivalent and alternative for substitution in forming conductive elements for electrical connection.

10. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uemura (6,331,450) and further of Yew et al (6,137,164).

Uemura teaches a method for forming a semiconductor device as applied to claims 1-3, 6,12,14,17,21,23-14 above.

Uemura already teaches forming the external conductive elements 240 of solder balls over the intermediate conductive elements 220, while claim 16 recites alternative technique for forming the external conductive elements by applying an anisotropically conductive film.

However, Yew teaches (at Figs 6A-6B; col 7, lines 4-38) an alternative technique for forming the external conductive elements by applying an anisotropic conductive film, wherein compression causes formation of the external conductive elements for electrically contacting between the two circuits.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the external conductive elements of Uemura by applying an anisotropic conductive film as taught by Yew et al. This is because of the desirability to form the external conductive elements for electrical connection between two circuits, wherein these alternative techniques art recognized equivalent and alternative for substitution in forming conductive elements for electrical connection.

Response to Arguments

11. Applicant's remarks filed July 11, 2003 have been fully considered but they are moot in view of the new ground(s) of rejection.

As shown in Figures 2A,2B,2E,2F,3A,3B,3F of Uemura (6,331,450), due to the existing of the recess channels form in the substrate, a pattern of light depressions is thus formed over the recess channels.

****

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.
Oacs

Michael Trinh
Primary Examiner